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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,690	01/16/2004	Richard L. Black	P/10-658	8450

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EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,690	BLACK, RICHARD L.	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C.102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> 102(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 4 & 8 are rejected under 35 U.S.C. §102(b) as being anticipated by Makaran (US 6630805).

Regarding claim 1 Makaran discloses an overcurrent protection circuit for a power switching transistor wherein the power switching transistor (Fig. 29 element 54 <MOSFET>) has a control electrode (Fig. 29 connection of the MOSFET to Rg) and two main electrodes (Fig. 29 connection of the MOSFET to L & C), the circuit comprising: a circuit including a protection switch for sensing the rate of change of voltage with respect to time (Fig. 29 element C) at one of the main electrodes of the power switching transistor and for controlling the protection switch (Fig. 29 elements Q1, Q2, D3 & Rp) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor if the rate of change exceeds a predefined value (col. 15 lines 5-10 <snubber: a device which senses and suppresses voltage transients - dv/dt>) the predefined value is inherent with the chosen components of the snubber.

Regarding claim 2 Makaran discloses the circuit of claim 1.
Makaran further discloses wherein the sensing circuit comprises a capacitor (Fig. 29 element C) coupled to a main electrode of the power switching transistor (Fig. 29 element 54 <MOSFET>) and a resistor (Fig. 29 element Rp) coupled to receive a pulse from said capacitor and for developing a voltage across the resistor to turn on the protection switch (Fig. 29 elements Q1 & Q2) if the voltage across the resistor exceeds the predefined value.

Regarding claim 3 Makaran discloses the circuit of claim 2.
Makaran further discloses wherein the protection switch comprises a transistor (Fig. 29 elements Q1 & Q2).

Regarding claim 4 Makaran discloses the circuit of claim 3.
Makaran further discloses wherein the protection switch comprises a bipolar junction transistor (Fig. 29 elements Q1 & Q2).

Regarding claim 8 Makaran discloses the circuit of claim 1.
Makaran further discloses wherein the power switching transistor comprises a field effect transistor (FET) (Fig. 29 element 54).

Claims 9, 10, 11 & 14 are rejected under 35 U.S.C. §102(b) as being anticipated by Turvey et al. (US 6759835

Regarding claim 9 Turvey et al. discloses an overcurrent protection circuit for a power switching transistor wherein the power switching transistor (Fig. 5 element TR1) has a control electrode (Fig. 5 element TR1 connected to Hi) and two main electrodes (Fig. 5 element TR1 connections to 28V Pos & L), the circuit comprising: a circuit comprising a protection transistor (col. 6 lines 4-10 & Fig. 4 element TR4). The circuit comprising an R-C circuit (Fig. 5 elements R7 & C4) for sensing the rate of change of voltage with respect to time at one of the main electrodes of the power switching transistor and for controlling the protection transistor (Fig. 4 element TR4) to remove a control signal to the control electrode of the power switching transistor to turn off the power switching transistor (col. 6 lines 18-26) if the rate of change exceeds a predefined value.

Regarding claim 10 Turvey et al. discloses the circuit of claim 9.
Turvey et al. further discloses wherein the R-C circuit comprises a capacitor (Fig. 5 element C4) coupled to a main electrode (Fig. 5 element C4 connected to TR1 through 28V Pos) of the power switching transistor and a resistor (Fig. 5 element R7 connected to C4) coupled to receive a pulse from said capacitor and for developing a voltage across the resistor to turn on the protection transistor (col. 6 lines 4-10 & Fig. 4 element TR4) if the voltage across the resistor exceeds the predefined value.

Regarding claim 11 Turvey et al. discloses the circuit of claim 10.
Turvey et al. further discloses wherein the protection transistor comprises a bipolar junction transistor (Fig. 4 element TR4).

Regarding claim 14 Turvey et al. discloses the circuit of claim 9.
Turvey et al. further discloses wherein the power switching transistor comprises a field effect transistor (FET) (Fig. 5 element TR1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a), which forms the basis for all obviousness rejections, set forth in this office action.

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 & 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Makaran (US 6630805) in view of Turvey et al. (US 6759835).

Regarding claim 5 Makaran discloses the circuit of claim 4.
Makaran does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor.
Turvey et al. teaches wherein the resistor is coupled across the base-emitter junction of the protection transistor (Fig. 1 element R6).
It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran device with the features of Turvey et al. because this configuration improves the sensing/controlling steps since it makes sure only variations in voltages (dv/dt) and not noise will activate the protection switch.

Regarding claim 6 Makaran discloses the circuit of claim 4.
Turvey et al. further teaches comprising a diode (Fig. 1 element D1) coupled across the base-emitter junction of the protection transistor to discharge the capacitor.

Claims 7 & 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Makaran (US 6630805) in view of Turvey et al. (US 6759835).

Regarding claim 7 Makaran discloses the circuit of claim 3.
Makaran does not disclose wherein the protection switch comprises a field effect transistor JFET.
Turvey et al. teaches wherein the protection switch comprises a field effect transistor JFET. (col. 2 lines 43-46).
It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran device with the features of Turvey et al. because FET's provide a cost effective solution while exhibiting good switching characteristics, and low "ON" resistance.

Regarding claim 12 Turvey et al. discloses the circuit of claim 11.
Turvey et al. does not disclose wherein the resistor is coupled across the base-emitter junction of the protection transistor.
It is known in the art that NPN or PNP transistor can be use depending upon considerations of design only. That is the resistor is coupled across the base-emitter junction of the protection transistor (col. 6 lines 4-10 & Fig. 4 element TR4<replacing transistor NPN for PNP>).

Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Turvey et al. (US 6759835) in view of Ohura et al. (US 5818281).

Regarding claim 13 Turvey et al. discloses the circuit of claim 10.
Turvey et al. does not disclose wherein the protection transistor comprises a field effect transistor (JFET).
Ohura et al. teaches wherein the protection switch comprises a field effect transistor JFET (Fig. 8 element 2).

It would have been obvious to a person with the skill in the art at the time the invention was made to modify the Makaran device with the features of Ohura.et al. because with this type of circuit arrangement, when the power switching transistor is in an OFF state, the gate of the MOSFET becomes biased such that the MOSFET is switched ON which leads to a short circuit between the gate and the emitter of the power switching transistor. Thereby, even if a large voltage of dV/dt is applied between the collector and the emitter of the power switching transistor, this does not wrongly change state from its OFF state.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.
Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luis E. Román
Patent Examiner
Art Unit 2836

LR/120505

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